REMARKS

Reconsideration of the application, in view of the following remarks is respectfully requested.

The Examiner rejects Claims 12, 15-21 under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. in view of Chin et al. The Examiner states that Kelly disclosed an arbitration circuit for an output port comprising a FIFO queue containing a head pointer and the Examiner specifically refers to column 4, lines 50-67 to store in a common memory for a plurality of ports and plurality of characterizing data for each packet received at an input port in the data portion of the packet is stored in the common memory.

This rejection is respectfully traversed. First of all, the Examiner has ignored those statements made in a previous response which showed that the statements made by the Examiner characterizing Kelly et al. are incorrect. To start with, the portion of column 4 referred to by the Examiner, lines 50-67 do not at all refer to a head pointer, but to a "header". Applicants went through a great deal of trouble to explain the difference the Examiner in the previous response which clearly shows that there is a distinct difference between the "header" of Kelly et al. and the "head pointer" in the present application. This portion of the previous response is repeated hereunder for the convenience of the Examiner:

As to the term "head pointer", the Examiner is confusing this with the term of "header" referred to in the portion of Column 4, Lines 50-65, recited by the Examiner. If you review the text in this section carefully, the only term that is used is "header" not "head pointer". The term "header" is defined in the PCI Express base specification, revision 1.0(a) as a set of fields that appear in front of a Packet that contain the information required to determine the characteristics and purpose of the Packet. We have taken the definition for the term "head pointer" from the United States Patent 7,124,241 which recites: The "head" pointer that defines the memory address where the Packet should first begin to be written into the memory banks. Also in United States Patent 4,543,626 it recites that in one embodiment, the work queued is located in the control memory (22) and defined by a head pointer (60) which points to or contains the address of the location in control memory containing the first control block in the stations work cue (58,…). For the Examiner's convenience, a copy of the specific portion of the patents reciting these definitions is attached hereto. Accordingly, the "head pointer" points to the head or beginning of the file or in this case the Packet when

it is stored in the memory. This is not at all equivalent to the "header" referred to in the Kelly et al patent, the Examiner's statement to the contrary notwithstanding.

Secondly, Kelly does not store packets in a common memory, as stated by the Examiner. In our previous response we quoted from Kelly, column 8, lines 40-65 which we now repeat below:

"Only a single input buffer set 831 is provided for handling traffic, per virtual channel, in the downstream path from the upstream port. Separate single input buffer sets 839 and 841 are provided at each of the downstream ports, per virtual channel for handling traffic in the upstream direction." (emphasis added)

Thus, as we previously stated, it is clear that Kelly et al. functions in terms of the prior art by requiring separate memories for the input port and for each of the two output ports. Furthermore, each of these memories has a separate buffer per virtual channel.

The Examiner states that Kelly shows a plurality of arbitration circuits coupled to the look-up table for selecting the next packet to be sent out corresponding to a preselected characterizing datum and she refers to column 9, lines 1-48.

However, looking at column 9, we find no reference to the term "head pointer" but we do find two recitations of the functioning of Kelly et al. which specifically rebuke the Examiner's claim that it anticipates the present invention or renders it obvious with combined Chin et al. At lines 10-15 it recites:

"…to allow for steering transactions flowing out of the input buffers toward target buffers at the appropriate target output ports. This non-blocking switch 833 allows transfers to occur between any two combination of ports of the switch while simultaneously allowing transfers to occur between any two other combinations of sets of two ports of the switch" (emphasis added).

It is clear that the information is stored in input buffers and then transferred by the switch to buffers in the target output ports, thus negating any idea of a common memory to be used both by the input ports and the output ports, as in the present invention. Furthermore, referring again to column 9, at lines 54-58, it recites:

"Managing only one input buffer set and only one output buffer set (per port per virtual channel) with improved ordering requirements is much less complex than

managing multiple input and output buffer sets (per port per virtual channel) which have a much more complex ordering…" (emphasis added).

Thus, it is clear from Kelly et al. itself, as recited in two portions of column 9, specifically referred to by the Examiner, that Kelly et al. functions completely differently than the Examiner has characterized it and teaches away from utilization of a single buffer for all the input ports and output ports to share, with only the head pointers being transferred.

The Examiner states that Kelly et al. discloses all of the limitations as above but does not explicitly disclose a FIFO queue containing a head pointer to store in a common memory for plurality of ports. The Examiner states that Chen et al. discloses a buffer controller manages the buffer memory by integrating a plurality of bit mask bits and a link list pointer to enhance the performance of the controller for buffer management. The Examiner specifically refers to Paragraphs 15 and 16. The Examiner states that a pointer points to an address of the link list to manage the buffer memory so it is improved operation efficiency and the cost of the hardware can be reduced greatly. She therefore concludes it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Chen's teaching of the Kelly system so as to provide a method for buffer management for improving the efficiency of buffer management and a controller thereof.

This rejection is respectfully traversed. Kelly teaches away from the utilization of a single memory shared by all the ports of the device. Accordingly, combining this with Chen which shows a buffer controller manager would result in a device which has a plurality of memories at each input port and each output port. Since Kelly states that it would require a separate buffer for each port per virtual channel, and since it is well known that PCI Express supports eight virtual channels, Kelly would require a minimum of 24 separate memories for the configuration discussed in Figure 8, whereas the present invention require only a single memory. Combining Kelly et al. with Chen et al. would result in a more efficient memory for each of those 24 separate memories, but 24 separate memories would still be required, because that is the clear teaching of Kelly et al. Furthermore, nothing in Figure 4 of Chen et al. shows the utilization of a single memory shared by plurality of ports with plurality of characterizing data of each packet

received in the input port and a arbitration circuit which is coupled to look-up table for selecting the next packet to be sent out corresponding to a preselected characterizing data. Accordingly, the combination of Kelly et al. with Chen et al. does not yield the present invention nor render it obvious.

Accordingly, Applicants believe that the application, as previously amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted by,
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